Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

4.1 XO3225

3.2 x 2.5 mm SMD
Crystal Oscillator

For Automotive | Pb Free | RoHS Compliant

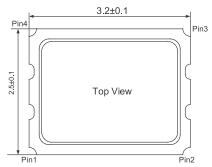
FEATURES

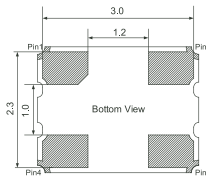
- Typical 3.2 x 2.5 x 1.0mm Ceramic SMD Package
- Tight Symmetry (45 to 55%) Available
- Operation Voltage: 1.35-5.5V
- Tri-State Enable/Disable Operation

TYPICAL APPLICATION

- SDH/SONET/WiMAX
- LTE and base station

DIMENSIONS





Pin Connection

Name	Connection
pin 1	Tri - State
pin 2	GND
pin 3	Fout
pin 4	Vdd

ELECTRICAL SPECIFICATION

Parameter		3.3V		2.5V		1.8V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		1	125	1	125	1	125	MHz
Standard Frequency		24, 26, 30, 40						MHz
Supply Current	At 15pF Load	—	25	—	25	—	20	mA
	No Load Condition, 1MHz≤F_O<10MHz	—	1.0	—	1.0	—	0.75	mA
	No Load Condition, 10MHz≤F_O<20MHz	—	1.0	—	1.0	—	0.75	mA
	No Load Condition, 20MHz≤F_O<80MHz	—	1.3	—	1.3	—	1.0	mA
	No Load Condition, 80MHz≤F_O<125MHz	—	6	—	6	—	3	mA
Duty Cycle		45	55	45	55	45	55	%
Output Level	Output High	2.97	—	2.25	—	1.62	—	V
	Output Low	—	0.33	—	0.25	—	0.18	
Transition Time: Rise/Fall Time+	1.25MHz≤F_O<10MHz	—	3	—	4	—	5	nSec
	10MHz≤F_O<20MHz	—	3	—	3	—	4	nSec
	20MHz≤F_O<80MHz	—	3	—	3	—	4	nSec
	80MHz≤F_O<125MHz		3		3		4	nSec
Startup Time		—	2	—	2	—	2	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	2.31	—	1.75	—	1.26	—	V
	Disable (Low Voltage or GND)	—	0.99	—	0.75	—	0.54	
Output Loading		15		15		15		pF
Stand by Current	(@-40 ~ 85°C)	—	10	—	10	—	10	uA
	(@-40 ~ 125°C)	—	20	—	20	—	20	uA
Aging (@25°C, 1st Year)		—	±3	—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	-55	125	°C
Period Jitter(Pk-Pk)		—	40	—	40	—	40	pSec
RMS Phase Jitter(Intergrated 12KHz ~ 20MHz)		—	1	—	1	—	1	pSec

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

FREQ. STABILITY vs. TEMP. RANGE

Temp.(℃) \ ppm	±20	±25	±50
-10 ~ +60	○	○	○
-20 ~ +70	△	○	○
-40 ~ +85	×	○	○

*o: Available Δ: Condition X: Not available
*Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration.

Note: not all combination of options are available. Other specifications may be available upon request.
Specifications subject to change without notice.

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

4.2 XO2520

2.5 x 2.0mm SMD CMOS Output Crystal Oscillator

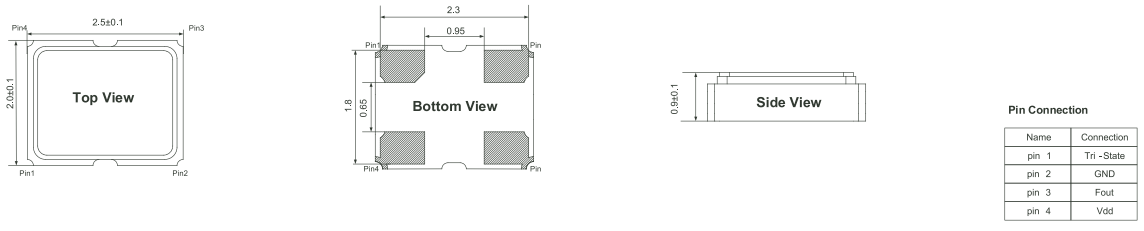
FEATURES

- Ultra Low Power Supply Voltage: 1.35-5.5V
- Low Noise Typical: 0.3 pS at 12 kHz ~ 20 MHz
  Supply Options Frequency Offsets
- Singled-end Output: CMOS
- Temperature Range: -40 ~ 85°C Operation
- Frequency Support from 1 MHz to 50MHz
- Pb-free/RoHS Compliant

TYPICAL APPLICATION

- IoT
- Game Console
- Smartphone
- Wearable Device
- Digital Camera
- Digital Consumer Electronics

DIMENSIONS



Pin Connection

Name	Connection
pin 1	Tri - State
pin 2	GND
pin 3	Fout
pin 4	Vdd

ELECTRICAL SPECIFICATION

Parameter		3.3V		2.5V		1.8V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		1	125	1	125	1	125	MHz
Supply Current	At 15pF Load	—	25	—	25	—	20	mA
	No Load Condition, 1MHz≤F_O<10MHz	—	1.0	—	1.0	—	0.75	mA
	No Load Condition, 10MHz≤F_O<20MHz	—	1.0	—	1.0	—	0.75	mA
	No Load Condition, 20MHz≤F_O<80MHz	—	1.3	—	1.3	—	1.0	mA
	No Load Condition, 80MHz≤F_O<125MHz	—	6	—	6	—	3	mA
Duty Cycle		45	55	45	55	45	55	%
Output Level	Output High	2.97	—	2.25	—	1.62	—	V
	Output Low	—	0.33	—	0.25	—	0.18	
Transition Time: Rise/Fall Time+	1.25MHz≤F_O<10MHz	—	4	—	3	—	3	nSec
	10MHz≤F_O<20MHz	—	3	—	3	—	3	nSec
	20MHz≤F_O<80MHz	—	2	—	2	—	2	nSec
Startup Time		—	4	—	4	—	4	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	0.7VDD	—	0.7VDD	—	0.7VDD	—	V
	Disable (Low Voltage or GND)	—	0.3VDD	—	0.3VDD	—	0.3VDD	

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

ELECTRICAL SPECIFICATION

Parameter		3.3V		2.5V		1.8V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Output Loading		15		15		15		pF
Stand by Current		—	100	—	100	—	100	uA
Aging (@25°C, 1st Year)		—	±3	—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	-55	125	°C
Phase Noise(Typ.)		Typ.	Max.	Typ.	Max.	Typ.	Max.	
At VDD=1.2V, Fout=24MHz	1 kHz offset	-130	—	-133	—	-135	—	dBc/Hz
	10 kHz offset	-140	—	-143	—	-143	—	
	100 kHz offset	-148	—	-150	—	-150	—	
	1 MHz offset	-152	—	-155	—	-155	—	
Period Jitter(Pk-Pk)		—	40	—	40	—	40	pSec
RMS Phase Jitter(Intergrated 12KHz ~ 20MHz)		—	1	—	1	—	1	pSec

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.
+ Transition times are measured between 20% and 80% of VDD.

FREQ. STABILITY vs. TEMP. RANGE

Temp.(°C) \ ppm	±20	±25
-10 ~ +60	○	○
-20 ~ +70	○	○
-40 ~ +85	△	○

*o: Available Δ: Condition X: Not available
*Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration.

Note: not all combination of options are available. Other specifications may be available upon request.
Specifications subject to change without notice.

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

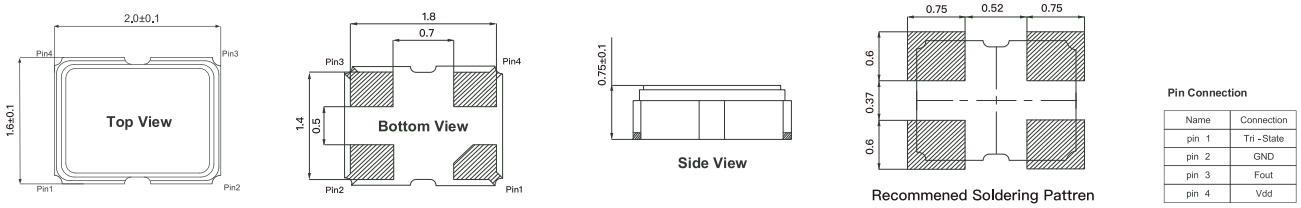
4.3 XO2016

2.0x1.6mm
CMOS Crystal Oscillator

FEATURES AND APPLICATIONS

-External Dimensions: 2.0x1.6x0.75 mm
-Small Size, High Reliability
-Wide Supply Voltage：1.7-3.6V
-Widely applied in industrial communication,navigation, radar, and other fields
-AEC-Q100&AEC-Q200 compliant

DIMENSIONS



ELECTRICAL SPECIFICATION

Specifications		3.3V		2.5V		1.8V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Operating Voltage(VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Output Frequency		1	125	1	125	1	125	MHz
Supply Current	At 15pF Load	—	25	—	25	—	20	mA
	When no load is provided, 1MHz≤F_O<10MHz	—	1.0	—	1.0	—	0.75	mA
	When no load is provided, 10MHz≤F_O<20MHz	—	1.0	—	1.0	—	0.75	mA
	When no load is provided, 20MHz≤F_O<80MHz	—	1.3	—	1.3	—	1.0	mA
	When no load is provided, 80MHz≤F_O<125MHz	—	6	—	6	—	3	mA
	Duty Cycle	45	55	45	55	45	55	%
Output Level	VoH	2.97	—	2.25	—	1.62	—	V
	VoL	—	0.33	—	0.25	—	0.18	
Transition Time: Rise/Fall Time+	1.25MHz≤F_O<10MHz	—	4	—	5	—	6	nSec
	10MHz≤F_O<20MHz	—	4	—	5	—	6	nSec
	20MHz≤F_O<80MHz	—	4	—	5	—	6	nSec
Start-up time		—	5	—	5	—	5	mSec
Tri-state (connect to Pin1)	On (High Level or Floating)	0.7VDD	—	0.7VDD	—	0.7VDD	—	V
	Off(Low Level or Ground)	—	0.3VDD	—	0.3VDD	—	0.3VDD	
Output Load		15		15		15		pF
Standby Current		—	100	—	100	—	100	uA
Aging(@25°C,the first year)		—	±3	—	±3	—	±3	ppm
Storage Temperature		-55	125	-55	125	-55	125	°C
Jitter(Vp-p)		—	40	—	40	—	40	pSec
Phase jitter Root-mean-square(12KHz～20MHz)		—	1	—	1	—	1	pSec

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

FREQ. STABILITY vs. TEMP. RANGE

Temp.(℃) \ ppm	±20	±25	±50
-10 ~ +60	○	○	○
-20 ~ +70	○	○	○
-40 ~ +85	△	○	○
-40 ~+125	×	×	○

*o: Available △: Available on condition X: Unavailable
Note：Not all components are available. We can supply other specifications on demand.

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

4.4 LV3225

3.2 x 2.5 mm SMD LVPECL/LVDS/ HCSL Crystal Oscillator

For Automotive · Pb Free · RoHS Compliant

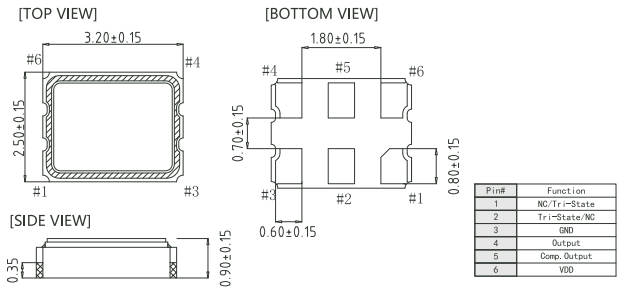
FEATURES

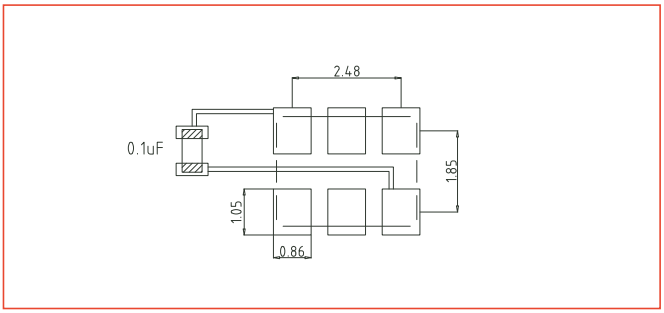
- Industry Standard 3.2 x 2.5 x 0.9 hermetically sealed ceramic package
- Very low jitter performance: typical 0.1 pS RMS from 12 kHz ~ 20 MHz
- Fundamental/3rd overtone crystal design
- Output frequency up to 250 MHz
- Tri-state enable/disable
- Up to 125°C operating temperature range

TYPICAL APPLICATION

- 10 Gbit Ethernet, Fiber Channel, Storage Area Network, SONET
- Enterprise Servers, Reference clocks for ADC and DAC
- Telecom

DIMENSIONS





ELECTRICAL SPECIFICATION

Parameter		LVPECL 3.3V Min.	LVPECL 3.3V Max.	LVPECL 2.5V Min.	LVPECL 2.5V Max.	LVDS 3.3V Min.	LVDS 3.3V Max.	LVDS 2.5V Min.	LVDS 2.5V Max.	Unit
Supply Voltage Variation (VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		10	250	10	250	10	250	10	250	MHz
Standard Frequency		25, 106.25, 125, 156.25, 161.1328, 212.5								
Supply Current	10MHz≤F_O<160MHz	—	75	—	75	—	50	—	50	mA
	160MHz≤F_O<250MHz	—	100	—	100	—	50	—	50	
Output Level	Output High	2.275	—	1.475	—	—	1.6	—	1.6	V
	Output Low	—	1.68	—	0.88	0.9	—	0.9	—	
Transition Time: Rise/Fall Time+		—	1	—	1	—	1	—	1	nSec
Startup Time		—	10	—	10	—	10	—	10	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	2.31	—	1.75	—	2.31	—	1.75	—	V
	Disable (Low Voltage or GND)	—	0.99	—	0.75	—	0.99	—	0.75	
Aging (@25°C, 1st Year)		—	±3	—	±3	—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	-55	125	-55	125	°C
Phase Noise @ 156.25 MHz	100 Hz	-95		-90		-90		-90		dBc/Hz
	1 kHz	-125		-125		-120		-120		
	10 kHz	-140		-140		-140		-140		
RMS Phase Jitter (Intergrated 12 KHz ~ 20MHz)	F_O<80MHz	—	1	—	1	—	1	—	1	pSec
	80MHz≤F_O<125MHz	—	0.5	—	0.5	—	0.5	—	0.5	
	125MHz≤F_O<170MHz	—	0.3	—	0.3	—	0.3	—	0.3	
	170MHz≤F_O<200MHz	—	0.5	—	0.5	—	0.5	—	0.5	
	200MHz≤F_O	—	0.3	—	0.3	—	0.3	—	0.3	

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

Parameter		HCSL				Unit
		3.3V		2.5V		
		Min.	Max.	Min.	Max.	
Supply Voltage Variation(VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		25	175	25	175	MHz
Standard Frequency		100				
Supply Current	25MHz≤F_O≤175MHz	—	50	—	50	mA
Output Level	Output High	0.6	—	0.58	—	V
	Output Low	—	0.15	—	0.15	
Transition Time: Rise/Fall Time+		—	0.5	—	0.5	nSec
Startup Time		—	10	—	10	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	0.7VDD	—	0.7VDD	—	V
	Disable (Low Voltage or GND)	—	0.3VDD	—	0.3VDD	
Aging (@25°C, 1st Year)		—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	°C
RMS Phase Jitter (Intergrated 12KHz ~ 20MHz)	25MHz≤F_O≤175MHz	—	0.5	—	0.5	pSec

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.
+ Transition times are measured between 20% and 80% of VDD.

FREQ. STABILITY vs. TEMP. RANGE

Temp.(°C) \ ppm	±25	±50
-10 ~ +60	○	○
-20 ~ +70	○	○
-40 ~ +85	△	○
-40 ~ +125	×	○

*o: Available Δ: Condition X: Not available
*Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration.

Note: not all combination of options are available. Other specifications may be available upon request.
Specifications subject to change without notice.

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

4.5 LV5032

5.0 x 3.2 mm SMD LVPECL/LVDS/ HCSL Crystal Oscillator

Pb Free

RoHS Compliant

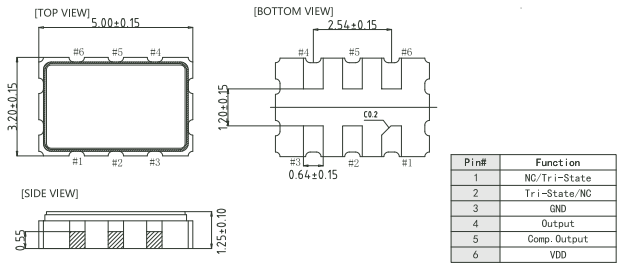
FEATURES

- Typical 5.0 x 3.2 x 1.25 mm hermetically sealed ceramic package
- Very low jitter performance: typical 0.3 pS RMS from 12 kHz ~ 20 MHz
- Fundamental/3rd overtone crystal design
- Output frequency up to 320 MHz
- Operating temperature up to 125°C
- Tri-state enable/disable

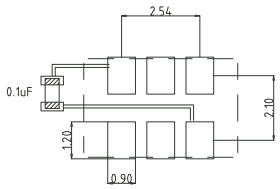
TYPICAL APPLICATION

- 10 Gbit Ethernet, Fiber Channel, Storage Area Network, SONET
- Enterprise Servers, Reference clocks for ADC and DAC
- Telecom

DIMENSIONS



Pin#	Function
1	NC/Tri-State
2	Tri-State/NC
3	GND
4	Output
5	Comp. Output
6	VDD



ELECTRICAL SPECIFICATION

Parameter		LVPECL 3.3V Min.	LVPECL 3.3V Max.	LVPECL 2.5V Min.	LVPECL 2.5V Max.	LVDS 3.3V Min.	LVDS 3.3V Max.	LVDS 2.5V Min.	LVDS 2.5V Max.	Unit
Supply Voltage Variation (VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		10	320	10	320	10	320	10	320	MHz
Standard Frequency		25, 106.25, 125, 156.25, 161.1328, 212.5								
Supply Current	10MHz≤F_O<160MHz	—	75	—	75	—	50	—	50	mA
	160MHz≤F_O<250MHz	—	100	—	100	—	50	—	50	
	250MHz≤F_O<320MHz	—	100	—	100	—	65	—	65	
Output Level	Output High	2.275	—	1.475	—	—	1.6	—	1.6	V
	Output Low	—	1.68	—	0.88	0.9	—	0.9	—	
Transition Time: Rise/Fall Time+		—	1	—	1	—	1	—	1	nSec
Startup Time		—	10	—	10	—	10	—	10	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	2.31	—	1.75	—	2.31	—	1.75	—	V
	Disable (Low Voltage or GND)	—	0.99	—	0.75	—	0.99	—	0.75	
Aging (@25°C, 1st Year)		—	±3	—	±3	—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	-55	125	-55	125	°C
Phase Noise @ 156.25 MHz	100 Hz	-95		-90		-90		-90		dBc/Hz
	1 kHz	-125		-125		-120		-120		
	10 kHz	-140		-140		-140		-140		
RMS Phase Jitter (Intergrated 12 KHz ~ 20MHz)	F_O<80MHz	—	1	—	1	—	1	—	1	pSec
	80MHz≤F_O<125MHz	—	0.5	—	0.5	—	0.5	—	0.5	
	125MHz≤F_O<170MHz	—	0.3	—	0.3	—	0.3	—	0.3	
	170MHz≤F_O<200MHz	—	0.5	—	0.5	—	0.5	—	0.5	
	200MHz≤F_O	—	0.3	—	0.3	—	0.3	—	0.3	

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

Parameter		HCSL				Unit
		3.3V		2.5V		
		Min.	Max.	Min.	Max.	
Supply Voltage Variation(VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		25	175	25	175	MHz
Standard Frequency		100				
Supply Current	25MHz≤F_o≤175MHz	—	50	—	50	mA
Output Level	Output High	0.6	—	0.58	—	V
	Output Low	—	0.15	—	0.15	
Transition Time: Rise/Fall Time+		—	0.5	—	0.5	nSec
Startup Time		—	10	—	10	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	0.7VDD	—	0.7VDD	—	V
	Disable (Low Voltage or GND)	—	0.3VDD	—	0.3VDD	
Aging (@25°C, 1st Year)		—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	°C
RMS Phase Jitter (Intergrated 12KHz ~ 20MHz)	25MHz≤F_o≤175MHz	—	0.5	—	0.5	pSec

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.
+ Transition times are measured between 20% and 80% of VDD.

FREQ. STABILITY vs. TEMP. RANGE

Temp.(°C) \ ppm	±25	±50
-10 ~ +60	○	○
-20 ~ +70	○	○
-40 ~ +85	△	○
-40 ~ +125	×	○

*o: Available Δ: Condition X: Not available
*Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration.

Note: not all combination of options are available. Other specifications may be available upon request.
Specifications subject to change without notice.

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

4.6 TLV5032

5.0 x 3.2 mm SMD LVPECL/LVDS Crystal Oscillator

Pb Free RoHS Compliant

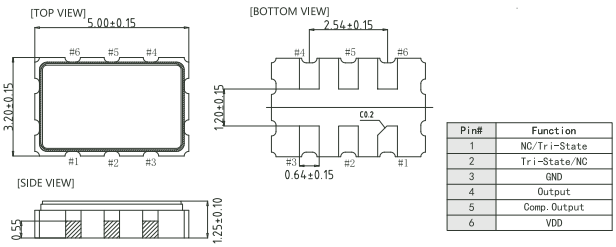
FEATURES

- Industry Standard 5.0 x 3.2 x 1.25 mm hermetically sealed ceramic package
- Very low phase jitter: < 1 pS (0.6 pS, typ.) RMS
- Tri-state enable/disable
- Fast delivery

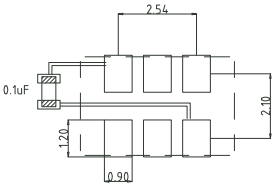
TYPICAL APPLICATION

- High-Speed Gigabit Ethernet, Fiber Channel, Storage Area Network, SONET
- Enterprise Server, SAS/SATA
- Microprocessors/DSP/FPGA
- Broadband Access
- Smart Grid

DIMENSIONS



Pin#	Function
1	NC/Tri-State
2	Tri-State/NC
3	GND
4	Output
5	Comp. Output
6	VDD



ELECTRICAL SPECIFICATION

Parameter		LVPECL 3.3V Min.	LVPECL 3.3V Max.	LVPECL 2.5V Min.	LVPECL 2.5V Max.	LVDS 3.3V Min.	LVDS 3.3V Max.	LVDS 2.5V Min.	LVDS 2.5V Max.	Unit
Supply Voltage Variation (VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		10	1500	10	1500	10	1500	10	1500	MHz
Standard Frequency		106.25, 125, 133.33, 150, 155.52, 156.25, 187.5, 212.5, 312.5, 622.08								
Supply Current	10MHz≤F_O<1500MHz	—	50	—	50	—	50	—	50	mA
Output Level	Output High	2.275	—	1.475	—	—	1.6	—	1.6	V
	Output Low	—	1.68	—	0.88	0.9	—	0.9	—	
Transition Time: Rise/Fall Time+		—	1	—	1	—	1	—	1	nSec
Startup Time		—	10	—	10	—	10	—	10	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	2.31	—	1.75	—	2.31	—	1.75	—	V
	Disable (Low Voltage or GND)	—	0.99	—	0.75	—	0.99	—	0.75	
Aging (@25°C, 1st Year)		—	±3	—	±3	—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	-55	125	-55	125	°C
Phase Noise @ 156.25 MHz	100 Hz	-85		-85		-85		-85		dBc/Hz
	1 kHz	-105		-105		-105		-105		
	10 kHz	-115		-115		-115		-115		
RMS Phase Jitter (Intergrated 12KHz ~ 20MHz)		—	1.5	—	1.5	—	1.5	—	1.5	pSec

+ Transition times are measured between 20% and 80% of VDD.

FREQ. STABILITY vs. TEMP. RANGE

Temp.(°C) \ ppm	±25	±50
-10 ~ +60	○	○
-20 ~ +70	○	○
-40 ~ +85	×	○

*o: Available Δ: Condition X: Not available
*Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration.

Note: not all combination of options are available. Other specifications may be available upon request.
Specifications subject to change without notice.

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

4.7 LV7050

7.0 x 5.0 mm SMD LVPECL/LVDS/HCSL Crystal Oscillator

Pb Free

RoHS Compliant

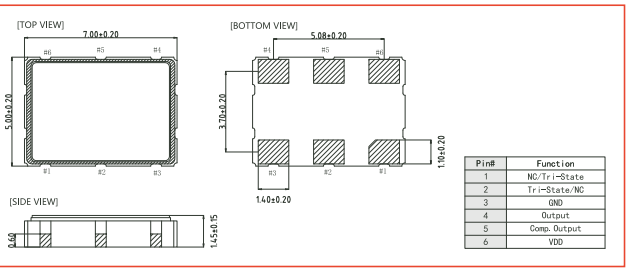
FEATURES

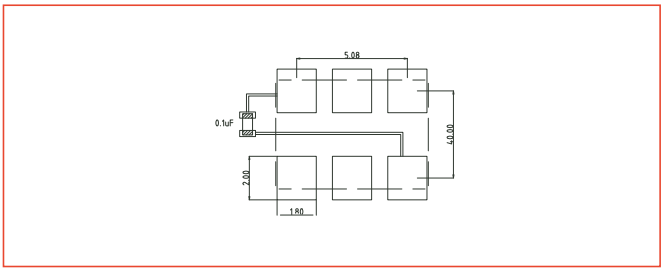
- Typical 7.0 x 5.0 x 1.45 mm hermetically sealed ceramic package
- Very low jitter performance: typical 0.3 pS RMS from 12 kHz ~ 20 MHz
- Fundamental/3rd overtone crystal design
- Output frequency up to 320 MHz
- Operating temperature up to 125°C
- Tri-state enable/disable

TYPICAL APPLICATION

- 10 Gbit Ethernet, Fiber Channel, Storage Area Network, SONET
- Enterprise Servers, Reference clocks for ADC and DAC
- Telecom

DIMENSIONS





ELECTRICAL SPECIFICATION

Parameter		LVPECL 3.3V Min.	LVPECL 3.3V Max.	LVPECL 2.5V Min.	LVPECL 2.5V Max.	LVDS 3.3V Min.	LVDS 3.3V Max.	LVDS 2.5V Min.	LVDS 2.5V Max.	Unit
Supply Voltage Variation (VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		10	320	10	320	10	320	10	320	MHz
Standard Frequency		77.76, 106.25, 125, 155.52, 156.25, 187.5, 212.5, 312.5								
Supply Current	10MHz≤F_O<160MHz	—	75	—	75	—	50	—	50	mA
	160MHz≤F_O<250MHz	—	100	—	100	—	50	—	50	
	250MHz≤F_O<320MHz	—	100	—	100	—	65	—	65	
Output Level	Output High	2.275	—	1.475	—	—	1.6	—	1.6	V
	Output Low	—	1.68	—	0.88	0.9	—	0.9	—	
Transition Time: Rise/Fall Time+		—	1	—	1	—	1	—	1	nSec
Startup Time		—	10	—	10	—	10	—	10	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	2.31	—	1.75	—	2.31	—	1.75	—	V
	Disable (Low Voltage or GND)	—	0.99	—	0.75	—	0.99	—	0.75	
Aging (@25°C, 1st Year)		—	±3	—	±3	—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	-55	125	-55	125	°C
Phase Noise @ 156.25 MHz	100 Hz	-100		-100		-100		-100		dBc/Hz
	1 kHz	-130		-130		-130		-130		
	10 kHz	-145		-145		-145		-145		
RMS Phase Jitter (Intergrated 12KHz ~ 20MHz)	F_O<80MHz	—	1	—	1	—	1	—	1	pSec
	80MHz≤F_O<125MHz	—	0.5	—	0.5	—	0.5	—	0.5	
	125MHz≤F_O<170MHz	—	0.3	—	0.3	—	0.3	—	0.3	
	170MHz≤F_O<200MHz	—	0.5	—	0.5	—	0.5	—	0.5	
	200MHz≤F_O	—	0.3	—	0.3	—	0.3	—	0.3	

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

Parameter		HCSL				Unit
		3.3V		2.5V		
		Min.	Max.	Min.	Max.	
Supply Voltage Variation(VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		25	175	25	175	MHz
Standard Frequency		100				
Supply Current	25MHz≤F_o≤175MHz	—	50	—	50	mA
Output Level	Output High	0.6	—	0.58	—	V
	Output Low	—	0.15	—	0.15	
Transition Time: Rise/Fall Time+		—	0.5	—	0.5	nSec
Startup Time		—	10	—	10	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	0.7VDD	—	0.7VDD	—	V
	Disable (Low Voltage or GND)	—	0.3VDD	—	0.3VDD	
Aging (@25°C, 1st Year)		—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	°C
RMS Phase Jitter (Intergrated 12KHz ~ 20MHz)	25MHz≤F_o≤175MHz	—	0.5	—	0.5	pSec

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.
+ Transition times are measured between 20% and 80% of VDD.

FREQ. STABILITY vs. TEMP. RANGE

Temp.(°C) \ ppm	±25	±50
-10 ~ +60	○	○
-20 ~ +70	○	○
-40 ~ +85	△	○
-40 ~ +125	×	○

*o: Available Δ: Condition X: Not available
*Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration

Note: not all combination of options are available. Other specifications may be available upon request.
Specifications subject to change without notice.

Oscillator (CMOS/LVPECL/LVDS/HCSL Output)

4.8 TLV7050

7.0 x 5.0 mm SMD LVPECL/LVDS Crystal Oscillator

Pb Free RoHS Compliant

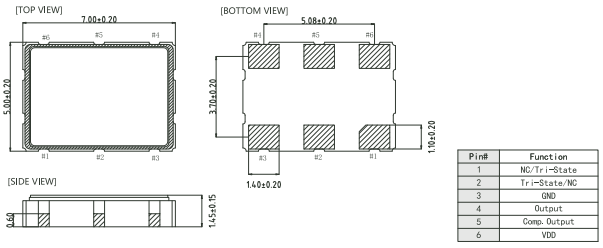
FEATURES

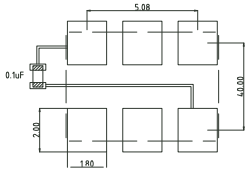
- Typical 7.0 x 5.0 x 1.45 mm hermetically sealed ceramic package
- Very low phase jitter : < 1 pS(0.6 pS, typ.) RMS
- Any frequency between 10 MHz and 1500 MHz
- Fast deliver
- Tri-state enable/disable

TYPICAL APPLICATION

- High-Speed Gigabit Ethernet, Fiber Channel, Storage Area Network, SONET
- Enterprise Server, SAS/SATA
- Microprocessors/DSP/FPGA
- Broadband Access
- Smart Grid

DIMENSIONS





ELECTRICAL SPECIFICATION

Parameter		LVPECL 3.3V Min.	LVPECL 3.3V Max.	LVPECL 2.5V Min.	LVPECL 2.5V Max.	LVDS 3.3V Min.	LVDS 3.3V Max.	LVDS 2.5V Min.	LVDS 2.5V Max.	Unit
Supply Voltage Variation (VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		10	1500	10	1500	10	1500	10	1500	MHz
Standard Frequency		106.25, 125, 133.33, 150, 155.52, 156.25, 187.5, 212.5, 312.5, 622.08								
Supply Current	10MHz≤F_O<1500MHz	—	50	—	50	—	50	—	50	mA
Output Level	Output High	2.275	—	1.475	—	—	1.6	—	1.6	V
	Output Low	—	1.68	—	0.88	0.9	—	0.9	—	
Transition Time: Rise/Fall Time+		—	1	—	1	—	1	—	1	nSec
Startup Time		—	10	—	10	—	10	—	10	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	2.31	—	1.75	—	2.31	—	1.75	—	V
	Disable (Low Voltage or GND)	—	0.99	—	0.75	—	0.99	—	0.75	
Aging (@25°C, 1st Year)		—	±3	—	±3	—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	-55	125	-55	125	°C
Phase Noise @ 156.25 MHz	100 Hz	-85		-85		-85		-85		dBc/Hz
	1 kHz	-105		-105		-105		-105		
	10 kHz	-115		-115		-115		-115		
RMS Phase Jitter (Intergrated 12KHz ~ 20MHz)		—	1.5	—	1.5	—	1.5	—	1.5	pSec

FREQ. STABILITY vs. TEMP. RANGE

Temp.(°C) \ ppm	±25	±50
-10 ~ +60	○	○
-20 ~ +70	○	○
-40 ~ +85	×	○

*o: Available Δ: Condition X: Not available
*Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration.

Note: not all combination of options are available. Other specifications may be available upon request.
Specifications subject to change without notice.